JAGVEER SINGH VERMA

Email: - (jagvirverma.ece@bitsindri.ac.in)
Mobile No. 09977500078

CAREER OBJECTIVE

An Electronics Engineer seeking a challenging position where technical competence is valued and where I can make a meaningful contribution to the growth of the Institute and can be a part of technological innovation.

WORK EXPERIENCE

Total experience: 18 years (Teaching + Research + Industrial)

1) Presently working as Assistant Professor on contract at **BIT SINDRI**, **Govt. Engineering College, Jharkhand** since Jan 2018 and **pursuing Ph.D. from IIT(ISM) Dhanbad**.
2) 6 years 4 months' work experience at Chouksey Engineering College, Bilaspur, Chhattisgarh (as Assistant Professor)
3) 3 years 9 months work experience at DIMAT, Raipur (as Senior Lecturer).
4) 1-year experience as a **Research Associate** under the esteemed guidance of **Dr M. Shojaei-Baghini (Professor, IIT Powai)** at **VLSI & Embedded System Design Center, SGIARC, Maharashtra.**
5) 1 year 8 months **Industrial experience** at URVI Transformers Wardha (M.S)

ACHIEVEMENTS

1) **Selected in TEQIP-III project under NPIU as Assistant Professor (With All India Rank of 26 in Electronics Engineering)**
2) **Best MTech project award (among SAARC) countries in VLSI Domain at Cadence design contest CDNlive 2006 under guidance of Professor Maryam Shojaei Baghini (IIT MUMBAI)**
3) Paper selected at **IASTED International Conference** on Circuits, Signals and Systems (ICCSS 2006), Nov20 to Nov 22, 2006, in San Francisco, USA.
4) Paper selected at **CDN Live! Conference, Santa Clara**, CA Sep 12 – 14, 2006
5) **Guided 6 M-Tech Thesis** in the area of **VLSI design.**
6) Worked as **Coordinator in 2 STTP at National Level at BIT Sindri.**

7) Conducted one-week National Level Workshop on VLSI design using Cadence tools in collaboration with **CADENCE** Bangalore.
8) GATE Scholarship **(GATE AIR 3870)**
9) National Open Merit scholarship after SSC.
10) **Administrative Responsibilities**: - NBA Coordinator, Asst. Hostel Superintendent, MIS Coordinator.

Letter of appreciation from **Director BIT Sindri** for helping other departments with **NBA work**.

SKILL SET

1) Good knowledge of Analog Circuit Design, Simulation & Layout Issues.
   Physical verification-DRC/LVS/RCX using Cadence Tools.
2) Operating system: - Red Hat Linux, Win Xp.
3) Software's Handled: - Xilinx,8051 ALP, MATLAB, PSPICE
4) Hardware used: - Spartan CPLD / FPGA kits

PERSONAL DETAILS

1) Name: -Jagveer Singh Verma
2) Date of Birth: - 04 Dec 1978
3) Father Name: - Mr. Ranjeet Singh Verma
4) Languages Known: -English, Hindi, Marathi
5) Marital Status: - Married
6) Permanent Address: -Type II, B-4, New Residential Colony, GGU Campus KONI, Bilaspur-445009

EDUCATIONAL DETAILS

S.No.	Degree / Education	Institute/University/ Board	Results
1	**Ph.D. (Pursuing)**	**IIT(ISM) Dhanbad**	**-**
2	M.E (Digital electronics) in **Distinction**	Amravati University (M.S)	75.12 %
3	B.E (Electronics)	Nagpur University (M.S)	61.44 %
4	H.S.C	Nagpur Board (M.S)	73.00 %
5	S.S.C	Nagpur Board (M.S)	82.71 %

Recent Symposium/ Workshop/Seminar/ Attended

Sl. No.	Title of Symposium/ Workshop/Seminar/Short–term Courses	Date	Organizing Institute
1	Faculty Development Programme	31st Jan to 4th Feb2018	IIT Madras
2	Refresher course on Research Methodology	16 June to 6 July 2018	GGV Central University Bilaspur
3	A I & Machine Learning	4 June to 8 June 2018	B.I.T Sindri
4	Outcome Based Education (OBE) & Accreditation	16 & 17 March 2018	B.I.T Sindri
5	Hands-on Introduction of HFSS in Microwave Applications	29th Oct to 2 Nov 2018	NIT Jamshedpur
6	Wireless and Mobile Communications	3rd Dec to 7th Dec 2018	BIT Sindri
7	32nd GISFI Standardization meeting on 5G	8th Dec to 9th Dec 2018	IETE, GISFI, IEEE & BSNL at ARTTC Ranchi
8	Advanced Pedagogy Digital Tool for TEQIP Faculty Members	10th June to 14th June 2019	IIT Kharagpur
9	Robotics and AI	24-28 June 2019	BIT Sindri
10	Digital Transformation in Teaching learning process	06-28 April 2020	IIT Mumbai
11	Basics of PLC	28 July -25th Aug 2020	BIT Sindri
12	Research Methods	18th -23th Jan 2021	IIM Bodh Gaya
13	Materials and Manufacturing: Insights to Modern Technologies (MMIMT-2022)	1st - 5th 2022	BIT Sindri

JOURNAL & CONFERENCE PAPERS

Journals papers

1) Review of Folded-Cascode and Telescopic Operational Amplifier,Journal of Emerging Technologies and Innovative Research JETIR ISSN-2349-5162,May 2017,Vol.4 ,Issue -05,Page 50-56,Achala Shukla ,Ankur Girolkar, Jagveer Verma

2) Design of Folded-Cascode operational Amplifier for High Frequency Application,International Journal of Scientific Progress and Research (IJSPR),ISSN-2349-4689,Vol.36,Issue 103,2017,Page 39-46,Achala shukla, Jagveer Verma

3) Design of an Operational Amplifier for sensor Interface, International Journal of scientific progress and research (IJSPR), ISSN-2349-4689,2017, Vol.36, Issue 103, Page 29-38, Ankur Girolkar,Jagveer Verma

4) Review of Sigma-Delta ADC, International journal of Advanced research in Electrical, Electronics and Instrumentation Engineering, Vol.5, Issue 4, April 2016, Sagar Chetani, Jagveer Verma,ISSN 2320-3765

5) Design of fully differential Telescopic op-amp with common mode feedback in 0.25um CMOS technology,International journal of Electrical and Electronics Engineering,2015,Volume 1 issue 1 ,page 32-37,Suman dewangan ,Jagveer Verma

6) FPGA Implementation of Simple and High Speed Vedic Multiplier, International journal of vlsi and signal processing Volume 2 issue 3-2015 Shilpi Thawait,Jagveer Verma ISSN no 2394-2584.

7) Analysis of ECG signal using base filter decomposition and threshold extraction,Internation journal of science and research, Volume 3 issue 12-2014,Mayank Yadu ,Jagveer Verma ISSN no. 2319-7064.

8) Scene understanding using back propagation by neural network, International Journal of Image Processing and Vision Sciences (IJIPVS) vol 1 issue 2, page 78-81,2012, Arti Tiwari, Jagveer Verma ISSN no .2278-1110.

Conference Papers

1) Design and Analysis of Two-Stage Op-Amp in 0.25um CMOS Technology, International Seminar on Non-Conventional Energy Sources for Sustainable Development of Rural Areas ,17 & 18 March 2016, Sagar Chetani,Jagveer Verma.

2) Design of low power operational transconductance amplifier (OTA) in 0.25um CMOS Technology,International conference on advanced research applications in engineering and technology,Shaastrarth 2015. 29-30 june 2015, Raghvendra Manikpuri, Jagveer verma.

3) 32 bit simple vedic multiplier, Interntional conference on advanced research applications in engineering and technology,Shaastrarth 2015. 29-30 june 2015, Shilpi Thawait, Jagveer Verma.

4) A review of signal processing Technique for wireless classification in medical applications, International conference on advanced research applications in engineering and technology, Shaastrarth 2014 ,23-24 March 2014 ,Mayank Yadu, Jagveer Verma.

5) Design of Ring Oscillator and LC oscillator in 0.18um CMOS Technology for GHz range applications, international conference on advanced research applications in engineering and technology, Shaastrarth 2014 ,23-24 March 2014, Kaustubh dubey, Jagveer Verma.

6) Overview on CMOS band gap reference, at National conference VIMARSH2013 ,12-13 sept 2013, Jagveer Verma.

7) Rapid advancement in wireless communication technology using cognitive radio on 4G communication, Nation conference, VIMARSH2013 ,12-13 sept 2013, Jagveer Verma.

8) Design of 3 stage ring oscillator in 0.18um CMOS technology for GHz range applications, at National conference VIMARSH2013 ,12-13 sept 2013, Kaustubh Dubey, Jagveer Verma.

9) Biometrics Technology in Public Distribution System, at National conference on Emerging Trends in Electronics and Telecommunication Engg. 27 Jan 2012, Jagveer Verma.

10) Design of low power OTA based FPAA in 0.35um CMOS process, accepted in **IASTED ICCSS** 2006, USA, Jagveer Verma

11) Design of FPAA using custom IC and optimization-based design flow. Proceedings of CDNlive 2006 USA, Jagveer Verma.

12) Design and implementation of low cost power optimized OTA based FPAA in 0.35um MM CMOS process.CDNlive 2006 India (**Winner of Cadence Design System,Inc .Design Contest Held among SAARC countries 2006**,Jagveer Verma.

13) Highly Programmable /Tunable cross-coupled OTA with High Tuning Range International conference on frontier technologies need for the industry business and education, ISTE chapter Adhiyamaan College of Engineering Hosur (T.N),Jagveer R.Verma.

Members of Professional Bodies

1) IEEE Member
2) ISTE Member